INTERFACING MEMORY AND I/O TO THE 20 MHZ Z8S180 SYSTEM

With speed requirements becoming increasingly critical, maximizing your system performance is key. Selecting the correct memory, peripherals, and glue logic speed is required to accomplish this goal.

GENERAL DESCRIPTION

As system speed increases, memory and I/O access time requirements become more critical. Attention needs to be paid to the access time of the memory and I/O. This application note outlines the speed requirement on memory and peripherals for the Z8S180 by using the Z8S18000ZCO Evaluation Board as a design example (Figure 3).

Note: (1) 20 MHz Z180™ timing is based on the Z80180/Z8S180 Product Specification.

(2) 20 MHz ESCC™ timing is based on the Z85230 Product Specification.

20 MHz Z180 System Requirements

Memory Requirement. Measured from Address Valid to Read Data Valid (Figure 1).

Note: EPROM and SRAM access times have to be less than 60 ns for zero wait state access.

Memory ADDR access time < T1 rising to T3 rising – T1 rising to Address valid – Data Read setup time
= 2 * Tcyc – tAD – tDRS
= 2(50) – 30 – 10
= 60 ns

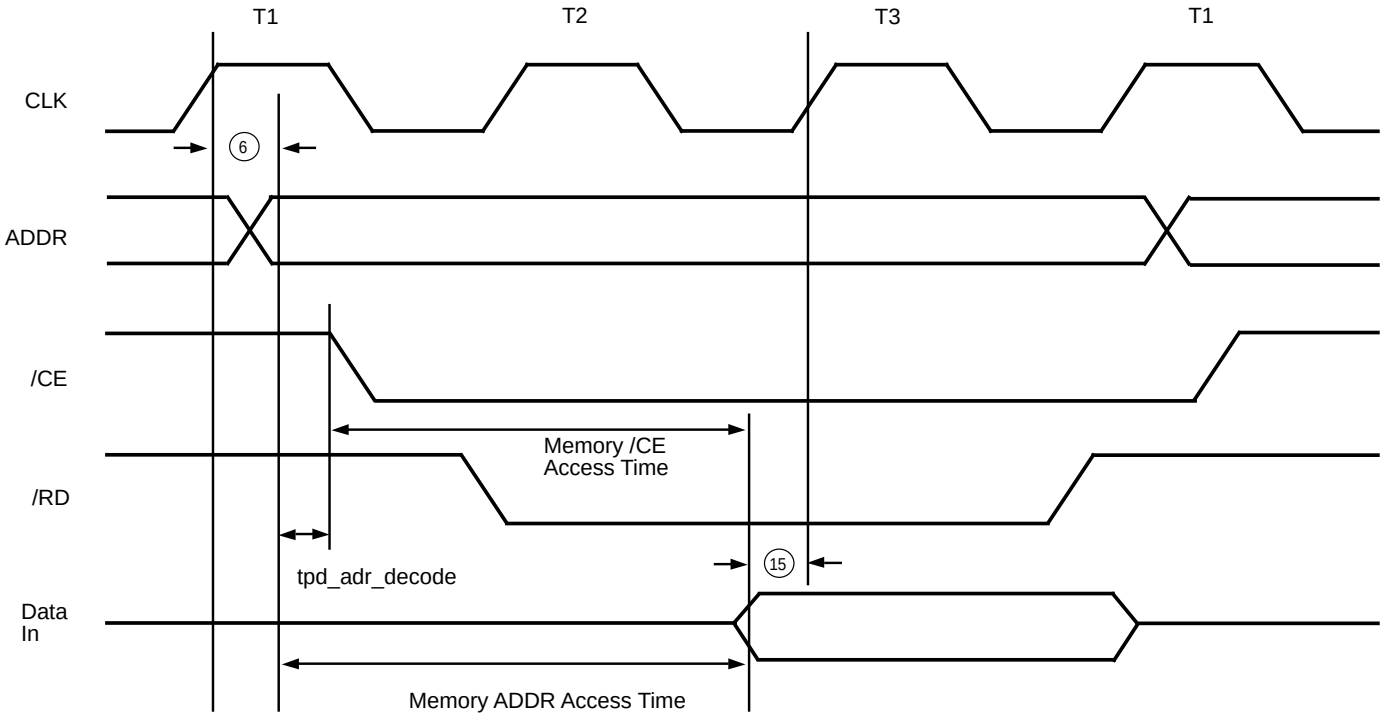
GENERAL DESCRIPTION (Continued)

Memory access time consists of two components:

- Memory /CE Access Time
- Address Decoding Propagation Delay, tpd_adr_decode

In some systems, /CE is derived from the Address Decoder Output. If propagation delay of the /CE address decoding logic is tpd_adr_decode, then Memory /CE Access Time = (60 – tpd_adr_decode) ns.

Propagation delay of a typical discrete address decoder, e.g., 74HC138 is 20 ns, the Memory /CE Access Time requirement is therefore 40 ns.



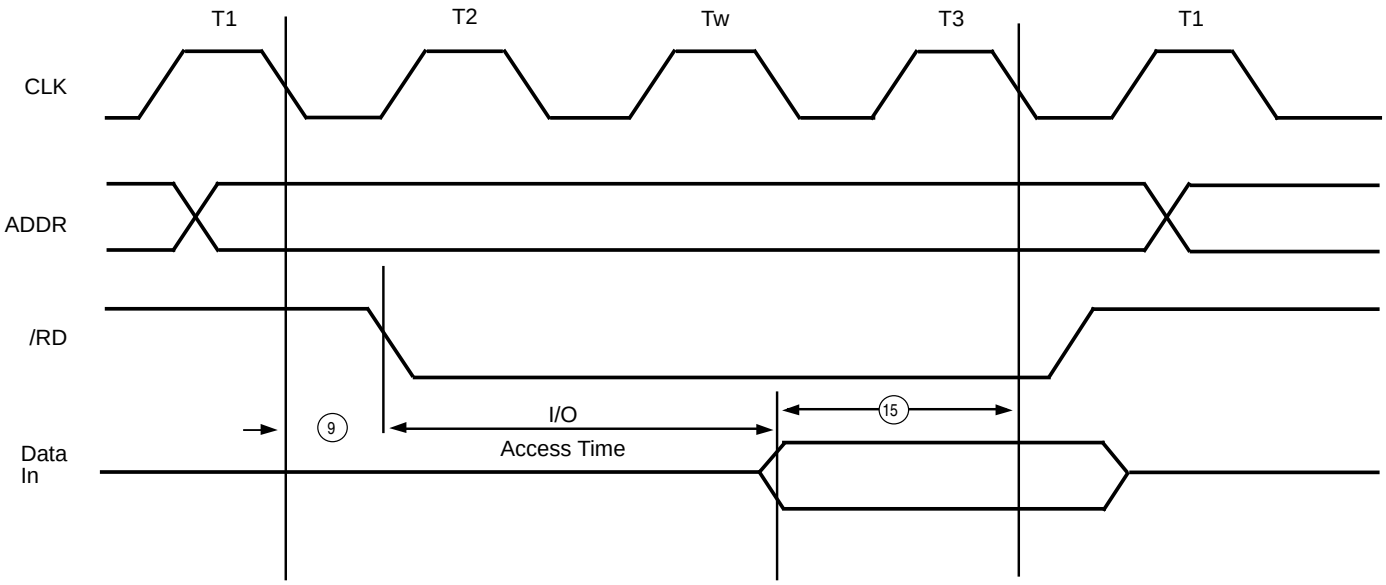
Spec 6: Address Valid from Clock Rise (tAD)
Spec 15: Data Read Setup Time (tDRS)

Figure 1. Z8S180 Memory Read Cycle Timing Analysis

Peripheral Requirement. Peripheral Read Cycle is measured from /RD Fall to Read Data Valid (Figure 2). Assume that /IORQ and /RD is used to decode I/O Read Cycle.

Note: I/O access time has to be less than 115 ns if one I/O wait state is programmed in DCNTL register during I/O cycle (IWI1 and IWI0 are "00").

I/O access time < T1 Fall to T3 Fall + Tw – T1 Fall to /RD Fall – Data Read setup time
= 3 * Tcyc – tRDD1 – tDRS
= 3(50) – 25 – 10
= 115 ns (1 wait state)



Spec 9: Clock Fall to /RD Fall (tRDD1)
Spec 15: Data Read Setup Time (tDRS)

Figure 2. Z8S180 Peripheral Read Cycle Timing Analysis

GENERAL DESCRIPTION (Continued)

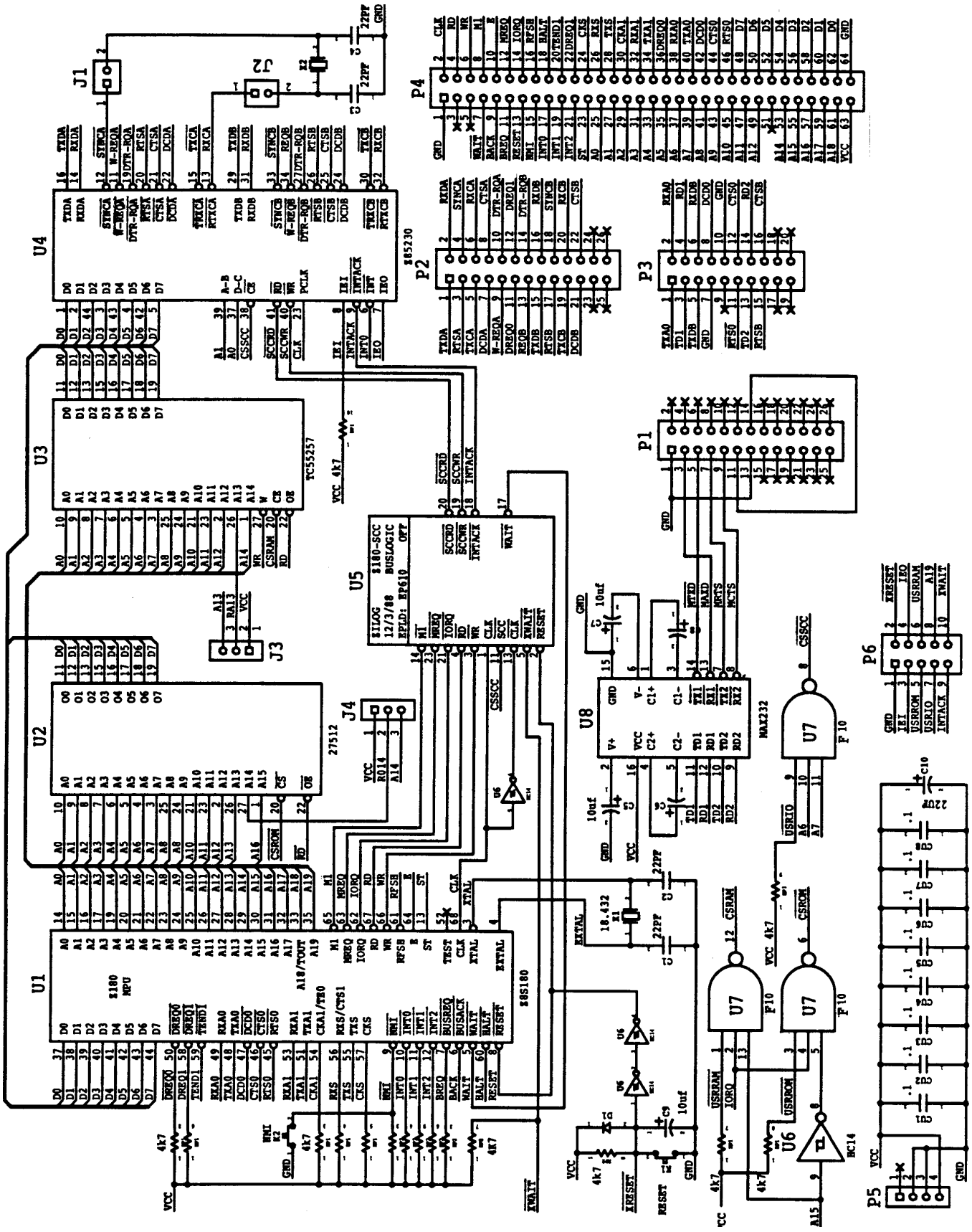


Figure 3. Z8S18000ZCO Evaluation Board Schematic

Interrupt Acknowledge Cycle. Assumes that /M1 is used for decoding Interrupt Acknowledge Cycle and /IORQ is used for initiating the interrupt vector read.

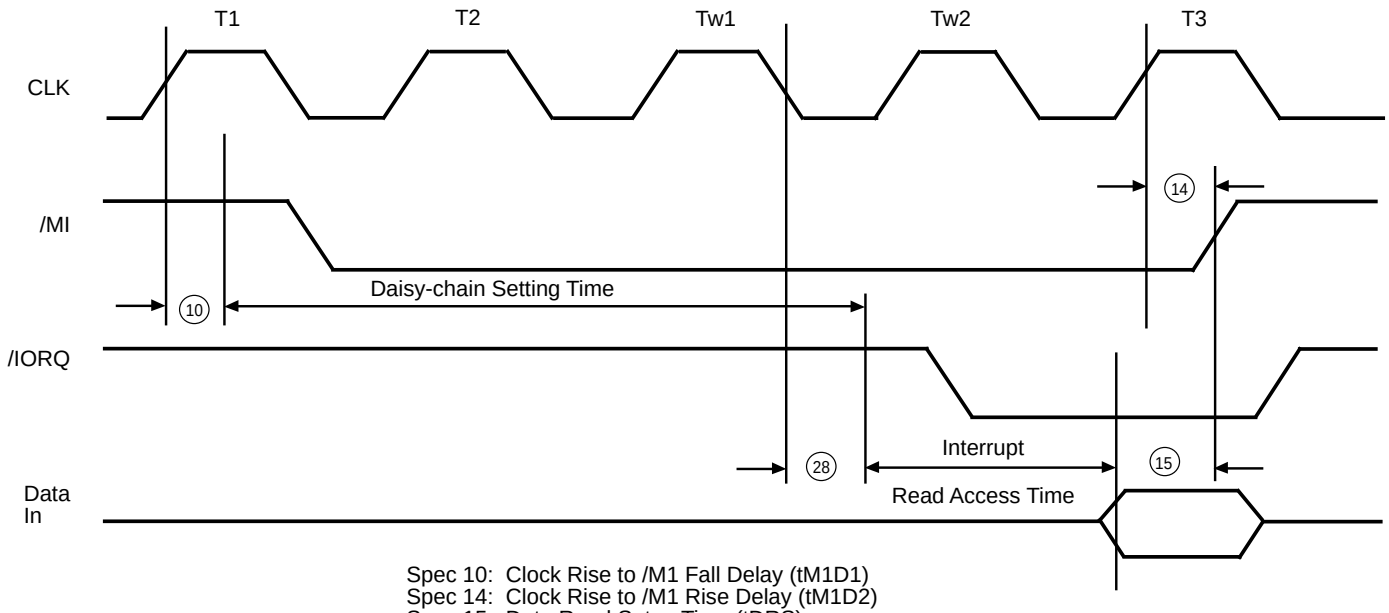
Daisy-Chain Settling Time. Measured from M1 Fall to /IORQ Fall (Figure 4).

= T1 Rise to Tw1 Fall – Clock Rise to /M1 Fall Delay + Clock Fall to /IORQ Fall Delay
= 2.5 * tcyc – tM1D1 + tIOD1
= 2.5(50) – 35 + 25
= 115 ns

Interrupt Vector Read Cycle Access Time. Measured from /IORQ Fall to Interrupt Vector Valid (Figure 4).

Note: Daisy-chain Settling Time must be less than 115 ns if two wait states are added in the interrupt acknowledge cycle. Interrupt Vector Read within 80 ns. The memory and I/O requirement at 20 MHz Z8S180 is summarized in Tables 1 and 2.

Interrupt read access time = Tw1 Fall to T3 Rise + Clock Rise to M1 Rise Delay
– Clock Fall to /IORQ Fall delay – Data Read Setup Time.
= 1.5 * tcyc + tM1D2 – tIOD1 – tDRS
= 75 + 40 – 25 – 10
= 80 ns



Spec 10: Clock Rise to /M1 Fall Delay (tM1D1)
Spec 14: Clock Rise to /M1 Rise Delay (tM1D2)
Spec 15: Data Read Setup Time (tDRS)
Spec 28: Clock Fall to /IORQ Fall Delay (tIOD1)

Figure 4. Z8S180 Interrupt Acknowledge Cycle Timing Analysis

GENERAL DESCRIPTION (Continued)

Table 1. Memory Access Requirements

MWI1: MWI0 of DCNTL	00	01	10	11
Memory Wait States	0 Wait	1 Wait	2 Wait	3 Wait
Memory Access Time (max)	60 ns	110 ns	160 ns	210 ns

Table 2. I/O Access Requirements

IWI1: IWI0 of DCNTL	00	01	10	11
I/O Wait States	1 Wait	2 Wait	3 Wait	4 Wait
I/O Access Time	115 ns	165 ns	215 ns	265 ns
INT0 Interrupt Acknowledge Cycle	2 Wait	4 Wait	5 Wait	6 Wait
Daisy-chain Settling Time	115 ns	215 ns	265 ns	315 ns
Interrupt Vector Read Access Time	80 ns	80 ns	80 ns	80 ns

DESIGN EXAMPLE USING THE Z8S180000ZCO EVALUATION BOARD

Memory Access

In the Z8S18000ZCO board, 27C512-75 (75 ns access time) EPROM is used. 74HC14 and 74F10 are used for memory decoding.

Since 60 ns (zero wait) < 99 ns < 110 ns (one wait), one memory wait state is programmed in Z8S18000ZCO.

Propagation delay in memory decoding logic = 19 (74HC14) + 5 (74f10) max
= 24 ns
Minimum access time in memory cycle = 24 + 75 ns
= 99 ns

I/O Access

I/O Read Cycle. In the Z8S18000ZCO board, 20 MHz ESCC is used and 74HCT10 is used for I/O decoding.

Minimum access time in I/O read cycle = 65 ns < 115 ns. Therefore, one wait state is good enough for normal I/O access.

ESCC, I/O access time = /RD Fall to Read Data Valid Delay
= 0 + 65
= 65 ns

Interrupt Acknowledge Cycle. Implementation of interrupt acknowledge cycle timing in Z8S18000ZCO is shown in Figure 5. The logic implementation is shown in Figure 6.

Tables 3 and 4 show the critical ESCC and Z8S180 timing in interrupt acknowledge cycle.

Table 3. Interrupt Acknowledge Cycle Timing Parameters (20 MHz ESCC)

Number	Symbol	Parameter	Min.	Max.
10	TsLA(PC)	/INTACK to PCLK Rise Setup Time	15 ns	
38	TdLAi(RD)	/INTACK to /RD Fall (ACK) Delay	45 ns	
40	TdRDA(DR)	/RD Fall (Ack) to Read Data Valid Delay		60 ns

DESIGN EXAMPLE USING Z8S190000ZCO (Continued)

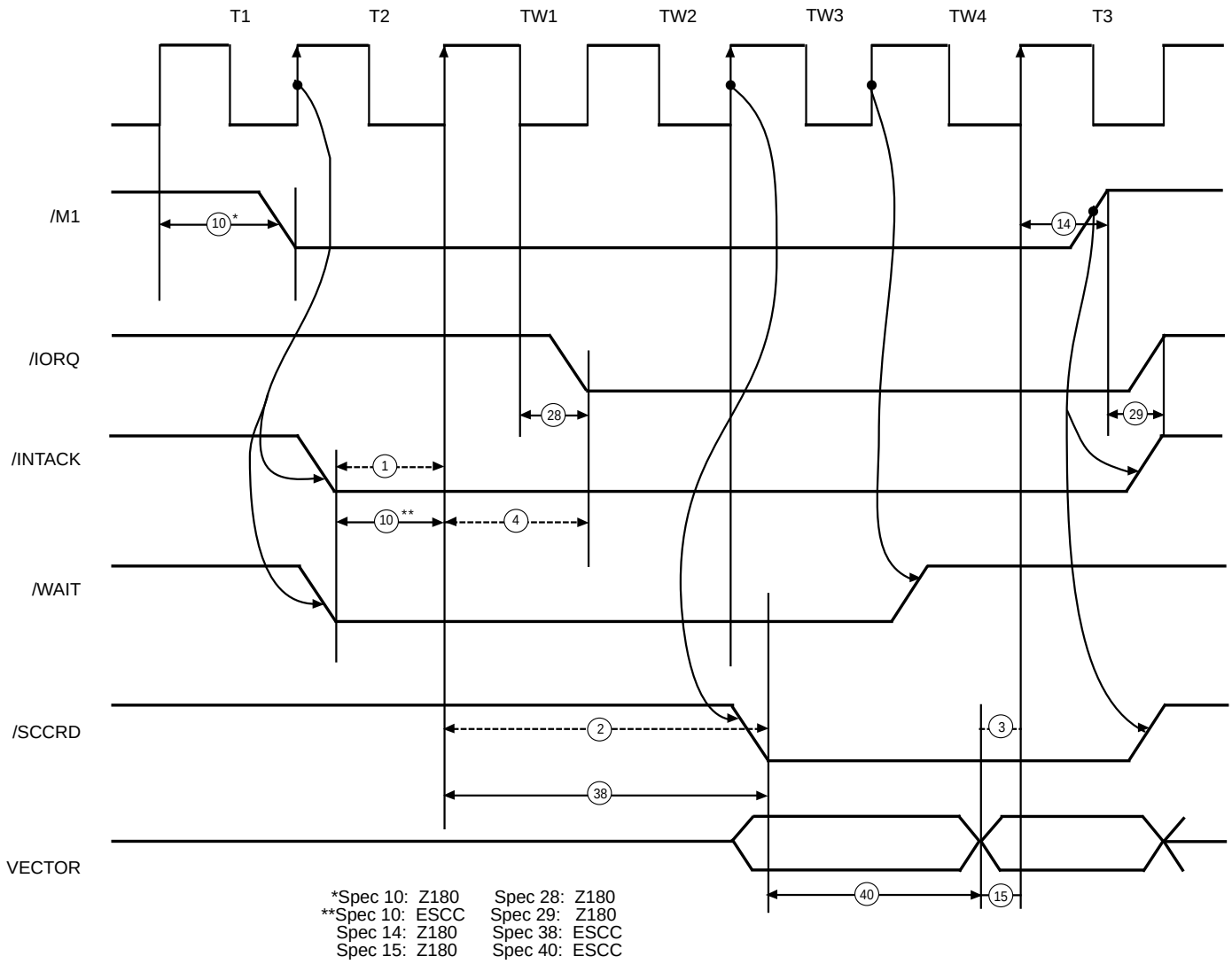


Figure 5. 20 MHz ESCC Interrupt Acknowledge Cycle Timing

Table 4. Interrupt Acknowledge Cycle Timing Parameters (20 MHz Z8S180)

Number	Symbol	Parameter	Min.	Max.
10	tM1D1	Clock Rise to /M1 Fall Delay		35 ns
14	tM1D2	Clock Rise to /M1 Rise Delay		40 ns
15	tDRS	Data Read Setup Time	10 ns	
28	tIOD1	Clock Fall to /IORQ Fall Delay		25 ns
29	tIOD2	Clock Fall to /IORQ Rise Delay		25 ns

State-Machine Approaches. The implementation requires a state-machine because ESCC requires synchronicity with the PCLK and also simple combinatory logic. Using /M1 to trigger /INTACK and /IORQ to trigger /SCCRD has a very tight margin in satisfying the timing requirements of the ESCC.

In the Z85230, the interrupt daisy-chain settling time takes a minimum of 45 ns (ESCC Spec 38), measured from the rising edge of Tw1. Since /IORQ is triggered from the falling edge of Tw1, the /IORQ falls with respect to the rising edge of Tw1 (Timing 4, Figure 5).

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=  0.5 * Tcyc + tIOD1 (Z180 Spec 28)
=  0.5 * 50 + 25
=  50 ns
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Therefore, although the settling time satisfies the ESCC requirements, very little margin is left. Additional I/O peripherals cannot be added on the interrupt daisy-chain.

Implementation of State-Machine. The objective of the state-machine is to:

- Provide enough setup time for ESCC to detect the interrupt acknowledgement from Z8S180 (Timing 1, Figure 5).
- Provide enough daisy-chain settling time for ESCC interrupt (Timing 2, Figure 5).
- Provide enough setup time for Z8S180 in sampling the interrupt vector (Timing 3, Figure 5).

Operation of State-Machine. The operation of the state-machine is as follows:

T1: Interrupt acknowledge cycle is detected when /M1 activates, but /MREQ remains inactive after the falling edge of T1.

T2: Interrupt acknowledge cycle is qualified when /MREQ is still inactive at the rising edge of T2. /INTACK and /WAIT are asserted upon the rising edge of T2.

Tw1: Activation of /INTACK is sampled by the ESCC at the rising edge of Tw1. /IORQ is activated at the falling edge of Tw1. However, this is irrelevant to the ESCC.

Tw2: Dummy wait state to allow enough daisy-chain settling time of ESCC. (Should be adjusted when another peripheral chip is used.)

Tw3: Read to ESCC, /SCCRD is asserted on rising edge of Tw3. ESCC is prepared to output the interrupt vector onto data bus.

Tw4: /WAIT is deactivated at the rising edge of Tw4 to conclude the additional wait states added in the interrupt acknowledge cycle. ESCC output the interrupt vector onto the data bus in this cycle.

T3: Z8S180 sample the interrupt vector at the rising edge of T3. Negates /M1 to conclude the Z8S180 interrupt acknowledge cycle. /INTACK and /SCCRD follow /M1 to terminate the ESCC interrupt acknowledge cycle.

DESIGN EXAMPLE USING Z8S190000ZCO (Continued)

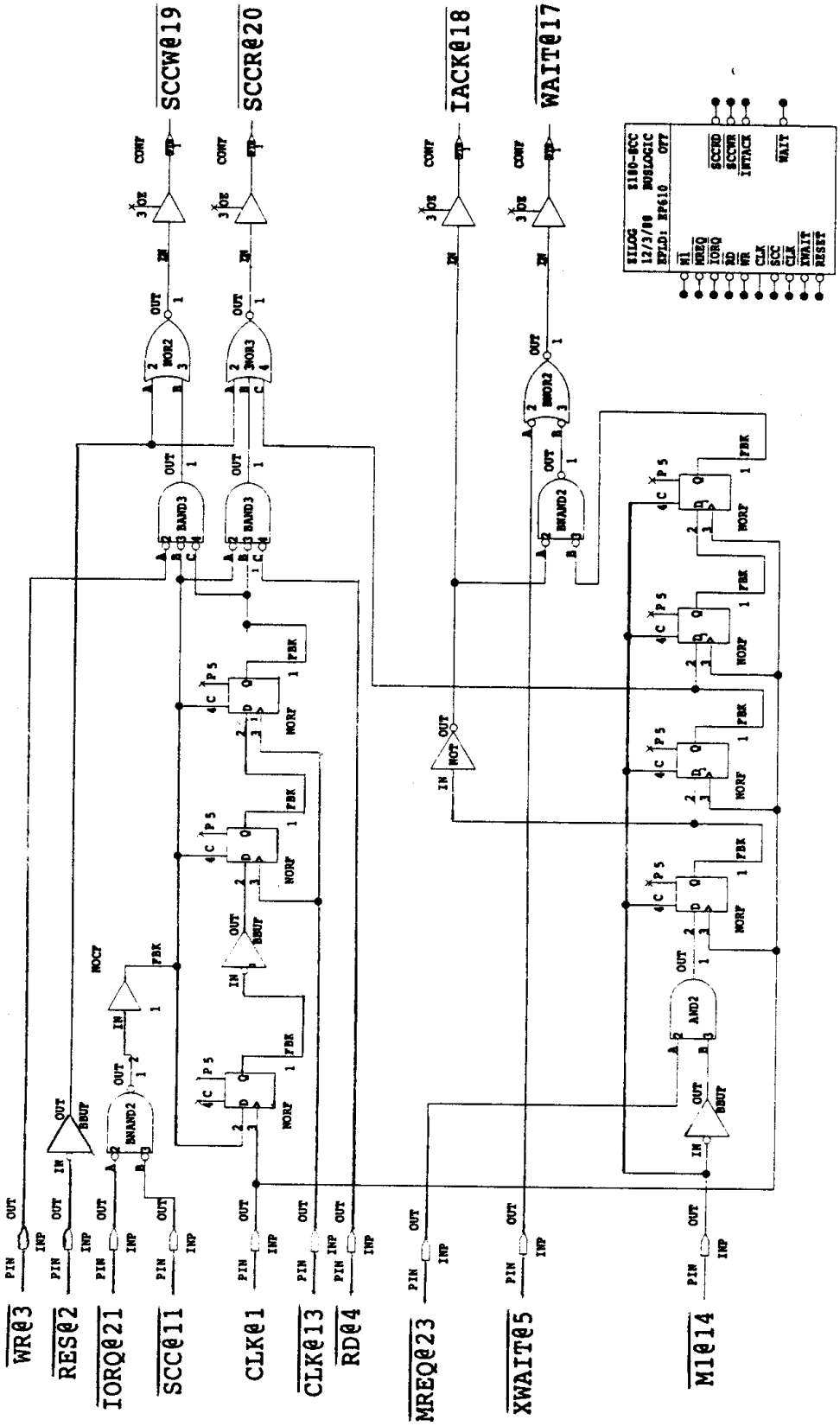

Figure 6. EPLD Circuit Implementation

Result of the State-Machine Implementation

#1: ESCC /INTACK to PCLK Setup Time

= Tcyc – T2 Rise to INTACK Fall Delay
= 50 – 25 (approx.)
= 20 ns > 15 ns (ESCC Spec 10, min.)

#2: ESCC Interrupt Daisy-Chain Settling Time

= 2 * Tcyc + Tw2 Rise to /SCCRD Delay
= 2 * (50) + 25
= 125 ns > 45 ns (ESCC Spec 38, min.)

#3: Z8S180 Interrupt Vector Read Setup Time

= 2 * Tcyc – Tw2 Rise to /SCCRD Delay – ESCC /RD Fall (Ack) to Read Data Valid Delay
= 2 * (50) – 25 – 60
= 15 ns > 10 ns (Z8S180 Spec 15, min.)

CONCLUSION

To maximize system performance, selecting the correct memory, peripherals, and glue logic speed is required. This application note describes the requirements in a 20 MHz Z8S180 system and has verified the Z8S18000ZCO design with the formulated requirement.

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